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# MORTEZA RAMEZANI

● PhD in Computer Science and Engineering ●

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## EDUCATION

**Pennsylvania State University**, University Park, U.S.A — 2015 – 2021 (expected)
PhD in Computer Science and Engineering

**Sharif University of Technology**, Tehran, Iran — 2009 – 2014
B.Sc. in Computer Engineering

## EXPERIENCES

**Research Assistant** — 6 years
I work as a research assistant in Computer System Lab (CSL) where my main focus is system optimization for graph processing and graph learning systems. Previously, I was part of DSN, working on reliability in high performance systems.

**Teaching Assistant** — 4 years
I served as a TA for several courses during my B.Sc and PhD. Selected courses:
**@ Penn State:** Machine Learning, System Programming, Computer Networks
**@ Sharif University:** Operating Systems, Computer Networks, Computer System,

**Software Developer** — 2 years
As a system software developer, I was implementing and building Sharif HPC clusters systems. Also, I worked as freelance web-developer, designing and deploying various websites, mainly using Python (Django) and PHP.

## PUBLICATIONS

Learn Locally, Correct Globally: A Distributed Algorithm for Training Graph Neural Networks — 2021
**Morteza Ramezani**, W. Cong, M. Mahdavi, A. Sivasubramaniam, M. Kandemir — *Under Review*

On Provable Benefits of Depth in Training Graph Convolutional Networks — 2021
W. Cong, **Morteza Ramezani**, M. Mahdavi — *Under Review*

On the Importance of Sampling in Training GCNs: Convergence Analysis and Variance Reduction — 2021
W. Cong, **Morteza Ramezani**, M. Mahdavi — *Under Review*

GCN meets GPU: Decoupling "When to Sample" from "How to Sample" — 2020
**Morteza Ramezani**, W. Cong, M. Mahdavi, A. Sivasubramaniam, M. Kandemir — ***NeurIPS***

GraphGuess: Approximate Graph Processing System with Adaptive Correction — 2020
**Morteza Ramezani**, A. Sivasubramaniam, M. Kandemir — *Arxiv*

Exploring the Impact of Memory Block Permutation on Performance of a Crossbar ReRAM Main Memory — 2017
**Morteza Ramezani**, N. Elyasi, M. Arjomand, M. Kandemir, A. Sivasubramaniam — ***IISWC***

CEDAR: Modeling Impact of Component Error Derating and Read Frequency on System-Level Vulnerability — 2014
H. Asadi, A. Haghdoost, **Morteza Ramezani**, N. Elyasi, A. Baniasadi — *Microelectronics Reliability*

## PROFESSIONAL ACTIVITIES

**Peer Reviews** — 5 years

- IEEE Transactions on Parallel and Distributed Systems
- International Symposium on High-Performance Computer Architecture (HPCA)
- International Symposium on Computer Architecture (ISCA)
- International Symposium on Performance Analysis of Systems and Software
- IEEE Transactions on Computers
- International Conference on Parallel Processing
- Principles and Practice of Parallel Programming